CSE303 Logic Design II – Tutorial 01

#	Student ID	Student Name	Grade (10)
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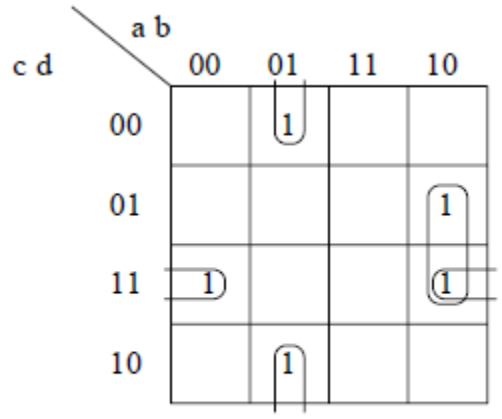
Q1

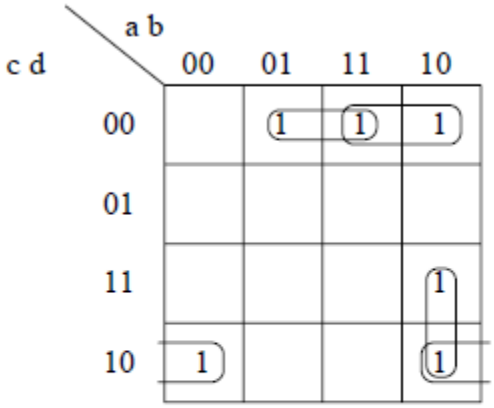
7.10 Find a minimum two-level, multiple-output AND-OR gate circuit to realize these functions.

$$f_1(a, b, c, d) = \Sigma\, m(3, 4, 6, 9, 11)$$
$$f_2(a, b, c, d) = \Sigma\, m(2, 4, 8, 10, 11, 12)$$
$$f_3(a, b, c, d) = \Sigma\, m(3, 6, 7, 10, 11) \quad \text{(11 gates minimum)}$$

Sol 1



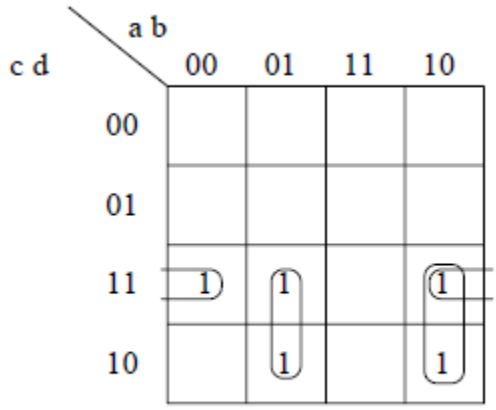
$f_1 = ab'd + b'cd + a'bd'$



$f_2 = ab'c + b'cd' + bc'd' + ac'd'$

$f_2 = ab'c + b'cd' + bc'd' + ab'd'$

11 gates



$f_3 = ab'c + b'cd + a'bc$

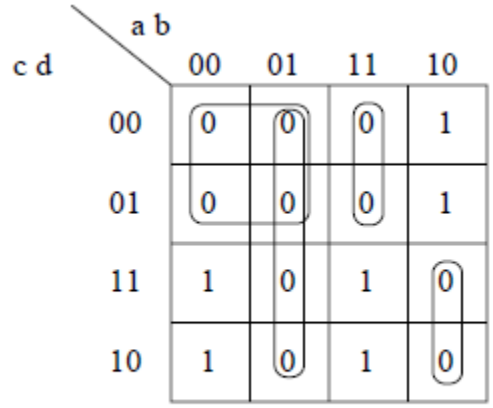
Q2

7.11 Find a minimum two-level OR-AND circuit to simultaneously realize

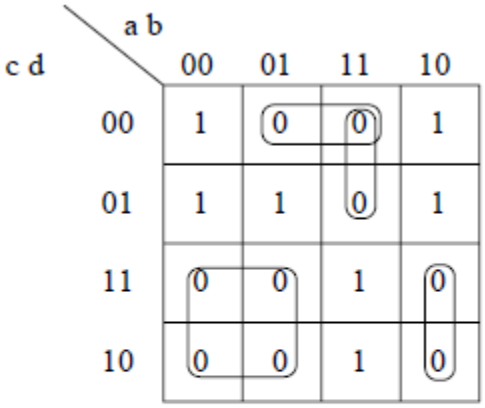
$$F_1(a, b, c, d) = \Sigma\, m(2, 3, 8, 9, 14, 15)$$
$$F_2(a, b, c, d) = \Sigma\, m(0, 1, 5, 8, 9, 14, 15)$$

(minimum solution has eight gates)

Sol 2



$F_1 = (a + c)(a + b')(a'+b'+c)(a'+b+c')$



$F_2 = (b'+c+d)(a'+b'+c)(a+c')(a'+b+c')$

$F_2 = (a+b'+d)(a'+b'+c)(a+c')(a'+b+c')$

8 gates