Logic Design I – Laboratory 01

Testing Inverter (Not) Gate (7804)

#	Student ID	Student Name	Grade (10)	Instructor signature
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2				

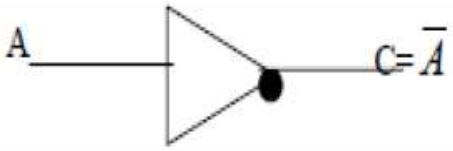
Delivery Date	

Objective

- To get familiar with ED100 logic design evaluation and testing kit.
- To test and verify the behavior of not gate.

Theory Overview

The basic logic gates are the building blocks of more complex logic circuits.
These logic gates perform the basic Boolean functions, such as Inversion.
Fig. below shows the circuit symbol of not gate, the small circle on the output of the circuit symbols designates the logic complement.

GATE	SYMBOL	INPUTS		OUTPUT
		A	B	C
NOT IC 7404		1	-	0
		0	-	1

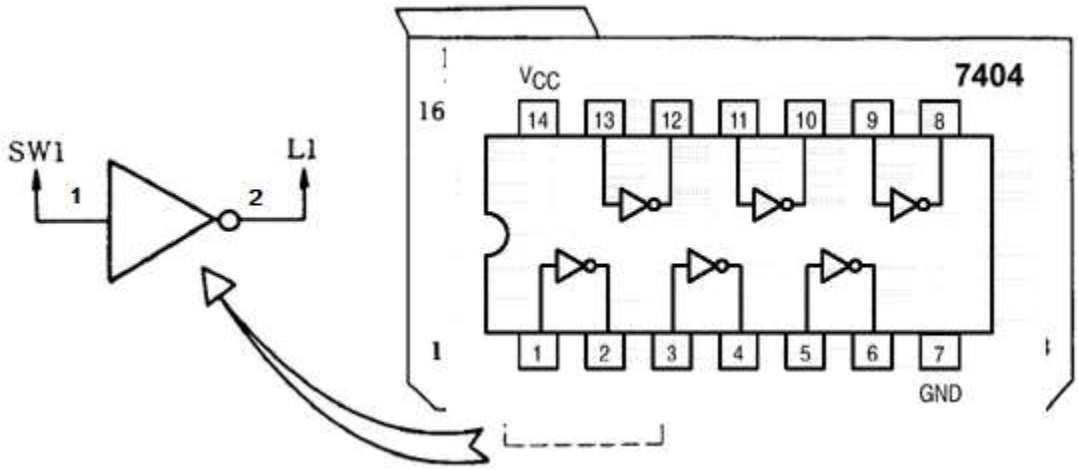
Digital IC gates are classified by family to which they belong.
Each logic family has its own basic electronic circuit upon which more complex digital circuits and functions are developed. The following logic families are the most frequently used;

TTL _Transistor-transistor logic
ECL _Emitter-coupled logic
MOS _Metal-oxide semiconductor
CMOS _Complementary metal-oxide semiconductor.

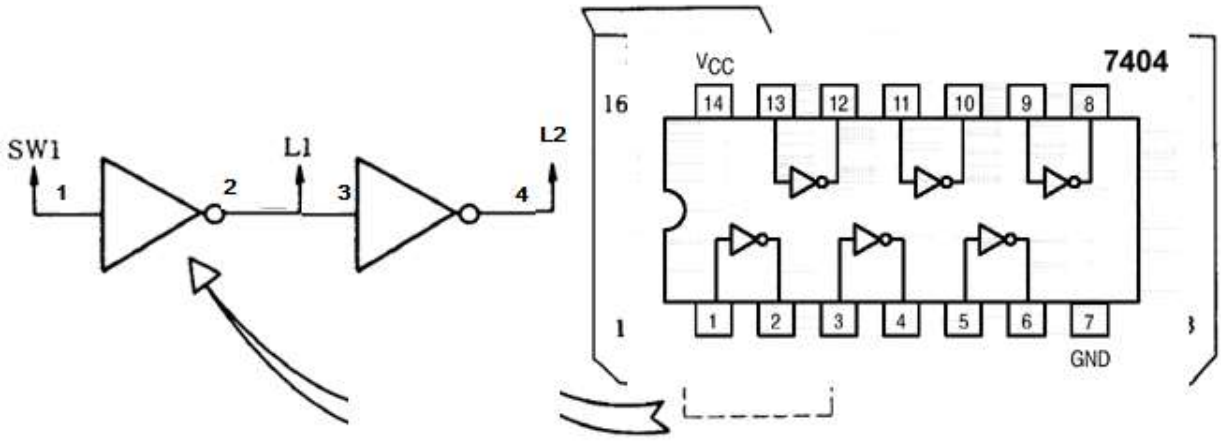
TTL and ECL are based upon bipolar transistors. TTL has a well-established popularity among logic families. ECL is used only in systems requiring high-speed operation. MOS and CMOS, are based on field effect transistors. They are widely used in large scale integrated circuits because of their high component density and relatively low power consumption. CMOS logic consumes far less power than MOS logic.
There are various commercial integrated circuit chips available. TTL ICs are usually distinguished by numerical designation as the 5400 and 7400 series.

Procedure

1. Insert a NOT gate [TTL 7404 #4-T] into the logic lab breadboard
2. Construct the circuit as shown in Fig

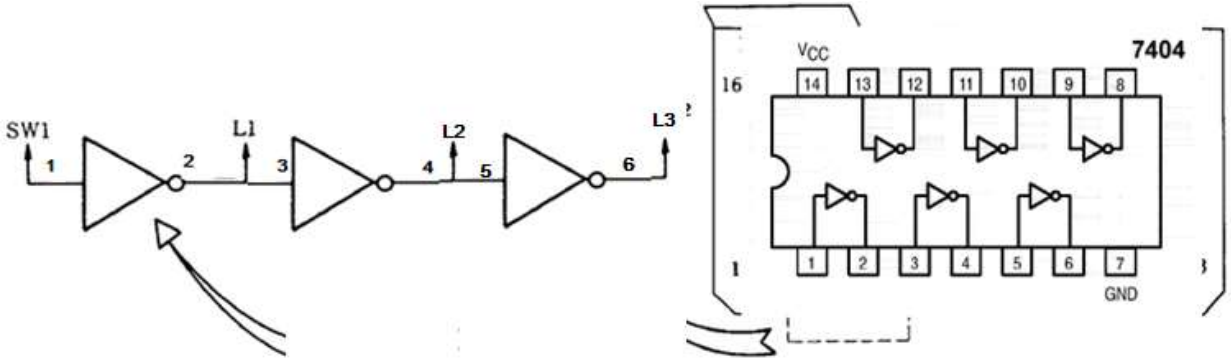


3. Set data switch SW1. Record the level of the output L1
4. Connect the output of first not gate as input to the next not gate, connect output to L2, as shown in figure



5. Set data switch SW1. Record the level of the output L1, L2

6. Connect the output of 2nd not gate as input to the next not gate, connect output to L3, as shown in figure



5. Set data switch SW1. Record the level of the output L1, L2, L3

Results and data analysis

Single note gate

Input (SW1)	Output (L1)
1	
0	

Two cascaded note gate

Input (SW1)	Output (L1)	Output (L2)
1		
0		

Three cascaded note gate

Input (SW1)	Output (L1)	Output (L2)	Output (L3)
1			
0			

Questions and Conclusions

1. What is the minimum number of gates needed to build a repeater or interface to a new circuit stage (detect the input signal and generate new clean signal)?

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2. In the two cascaded not cages, use voltmeter to measure the input voltage value and the final output voltage level? Is the output voltage level is the same as input voltage? Justify your answer?

Input (volt)	Final Output (volt)

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