EE 1st Projects – 2nd semester – spring 2016

Semester Project

#	Student ID	Student Name	Grade (10)
1			
2			
3			

Delivery Date	

Objective

Is to build a fully functional digital clock.

Theory of operation

The clock consists of two sections—minutes, hours and after reading the time 23 hours 59 minutes it resets back to 00.00, better referred to as the 0th hour.
It is evident from the block diagram that for Minute section we require a BCD Decade Counter for the unit's place and a Mod 6 counter for the ten's place, which means unit's place counting from 0-9-0 and repeats whereas the ten's place counts from 0-5-0 and repeats.
For the Hour section we require the counter for the unit's place to count 0-3-0 and for the ten's place it counts 0-2-0 and repeats

Circuit stages

The entire project has been divided into four modules. They are as follows:.

Power source

- 7805 regulator, to make sure a regulated 5 Volt is supplied to the circuit.

The clock section

- Using 555 timer as multivibrator circuit. You need to select R, C combination to ensure that.

$$T = 1.4\ R\ C$$

- For debugging purpose, you may build a variable clock generator (100k variable resistor, and 10 uF capacitor) 0 ~ 1.4 sec

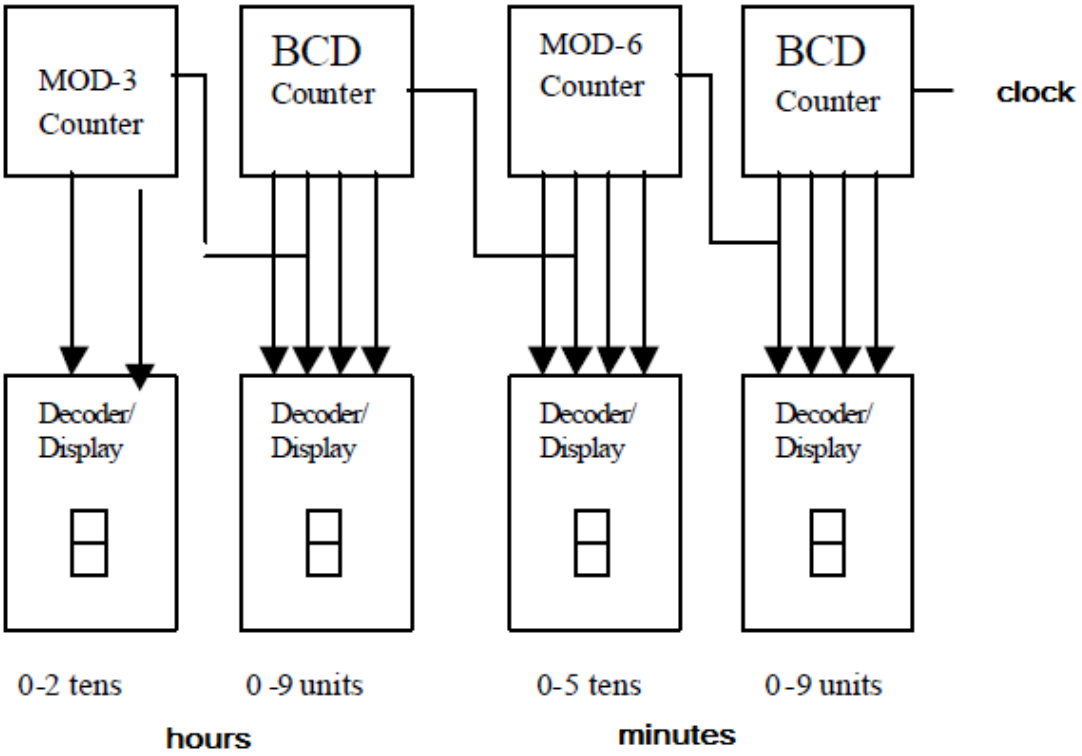
Minute section

- Using two counter ICs (IC 7490) in such a way that this portion produces output from 00 to 59 continuously with a frequency of 60Hz (1ppM).
- Using Driver IC (IC 7447) and seven-segment display to display the counts. Both the ICs are of common anode type.

Hour section

- Designing the circuit in such a way so that the output resets to 00 automatically displaying 23.59
- Here the counting proceeds with a frequency of one pulse per hour.

Block diagram



Components list

#	item	description	Quantity
1	……	……	……
2	……	……	……
3	……	……	……
4	……	……	……
5	……	……	……
6	……	……	……
7	……	……	……
8	……	……	……
9	……	……	……
10	……	……	……
11	……	……	……
12	……	……	……
13	……	……	……
14	……	……	……
15	……	……	……
16	……	……	……
17	……	……	……
18	……	……	……
19	……	……	……
20	……	……	……

Schematic diagram of power source stage

Schematic diagram of clock stage

Schematic diagram of minute's stage

Schematic diagram of hour's stage

Layout of whole circuit