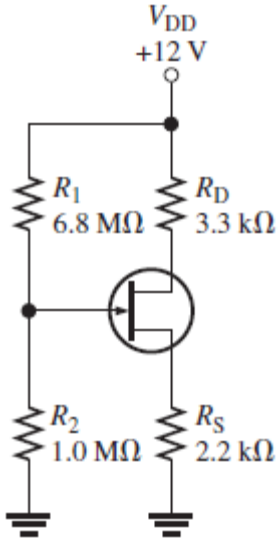
Electronic Circuits II - Tutorial 08

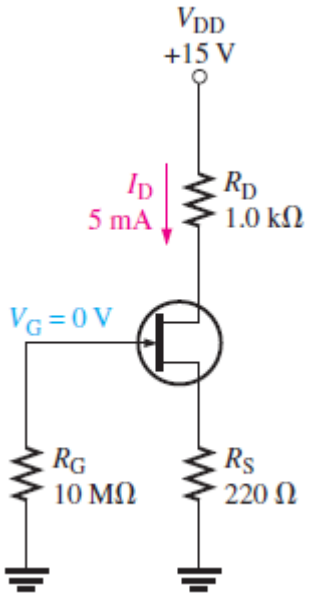
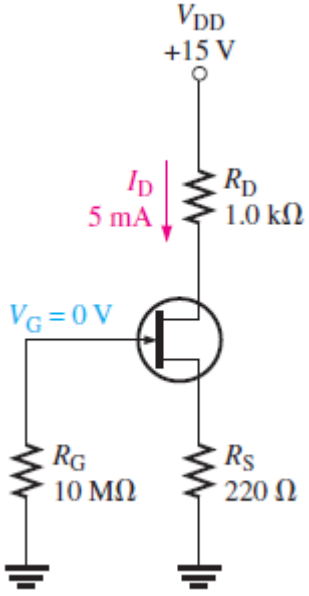
T & F

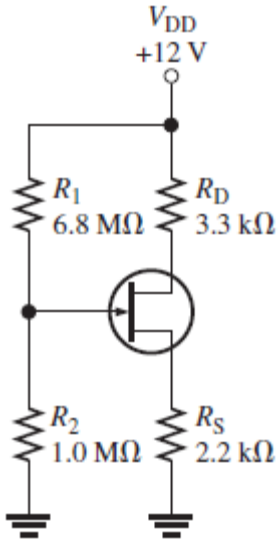
#		
1	The JFET always operates with a reverse-biased gate-to-source *pn* junction.	T
2	The channel resistance of a JFET is a constant.	F
3	The gate-to-source voltage of an *n*-channel JFET must be negative.	T
4	I_D becomes zero at the pinch-off voltage.	F
5	V_{GS} has no effect on I_D.	F
6	$V_{GS(off)}$ and V_P are always equal in magnitude but opposite in polarity.	T
7	The JFET is a square-law device because of the mathematical expression of its transfer characteristic curve	T
8	Forward transconductance is the change in drain voltage for a given change in gate voltage.	F

MCQ

#	Question	Answer
1	**1.** The JFET is **(a)** a unipolar device **(b)** a voltage-controlled device **(c)** a current-controlled device **(d)** answers (a) and (c) **(e)** answers (a) and (b)	e
2	The channel of a JFET is between the **(a)** gate and drain **(b)** drain and source **(c)** gate and source **(d)** input and output	b
3	A JFET always operates with **(a)** the gate-to-source *pn* junction reverse-biased **(b)** the gate-to-source *pn* junction forward-biased **(c)** the drain connected to ground **(d)** the gate connected to the source	a
4	I_{DSS} is **(a)** the drain current with the source shorted **(b)** the drain current at cutoff **(c)** the maximum possible drain current **(d)** the midpoint drain current	c
5	Drain current in the constant-current region increases when **(a)** the gate-to-source bias voltage decreases **(b)** the gate-to-source bias voltage increases **(c)** the drain-to-source voltage increases **(d)** the drain-to-source voltage decreases	a

6	A certain JFET datasheet gives $V_{GS(off)} = -4$ V. The pinch-off voltage, V_P, (a) cannot be determined (b) is −4 V (c) depends on V_{GS} (d) is +4 V	d
7	The JFET in Question 6 (a) is an *n* channel (b) is a *p* channel (c) can be either	a
8	For a certain JFET, $I_{GSS} = 10$ nA at $V_{GS} = 10$ V. The input resistance is (a) 100 MΩ (b) 1 MΩ (c) 1000 MΩ (d) 1000 MΩ	C
9	 If the value of *R*D in Figure is increased, *I*D will **(a)** increase **(b)** decrease **(c)** not change	b
10	For a certain *p*-channel JFET, *V*GS(off) = 8 V. The value of *V*GS for an approximate midpoint bias is **(a)** 4 V **(b)** 0 V **(c)** 1.25 V **(d)** 2.34 V	d
11	The drain-to-source resistance in the ohmic region depends on **(a)** *V*GS **(b)** the Q-point values **(c)** the slope of the curve at the Q-point **(d)** all of these	d

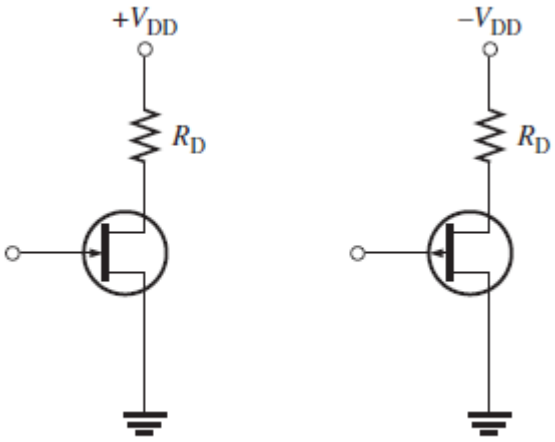
12	If the drain current in Figure 8–17 is increased, V_{DS} will  **(a)** increase **(b)** decrease **(c)** not change	
13	If the drain current in Figure is increased, V_{GS} will  **(a)** increase **(b)** decrease **(c)** not change	

14	For V_{GS} _ 0 V, the drain current becomes constant when V_{DS} exceeds **(a)** cutoff **(b)** V_{DD} **(c)** V_P **(d)** 0 V	a
15	The constant-current region of a FET lies between **(a)** cutoff and saturation **(b)** cutoff and pinch-off **(c)** 0 and I_{DSS} **(d)** pinch-off and breakdown	c
16	In a certain FET circuit, $V_{GS} = 0$ V, $V_{DD} = 15$ V, $I_{DSS} = 15$ mA, and $R_D = 470\ \Omega$. If R_D is decreased to 330 Ω, I_{DSS} is (a) 19.5 mA (b) 10.5 mA (c) 15 mA (d) 1 mA	c
17	At cutoff, the JFET channel is (a) at its widest point (b) completely closed by the depletion region (c) extremely narrow (d) reverse-biased	b
18	 If the value of $R2$ in Figure is decreased, V_G will **(a)** increase **(b)** decrease **(c)** not change	b
19	In a self-biased JFET, the gate is at **(a)** a positive voltage **(b)** 0 V **(c)** a negative voltage **(d)** ground	b

20	To be used as a variable resistor, a JFET must be **(a)** an *n*-channel device **(b)** a *p*-channel device **(c)** biased in the ohmic region **(d)** biased in saturation	c
21	When a JFET is biased at the origin, the ac channel resistance is determined by **(a)** the Q-point values **(b)** V_{GS} **(c)** the transconductance **(d)** answers (b) and (c)	d

Problems

Q1	Why must the gate-to-source voltage of an *n*-channel JFET always be either 0 or negative?
Sol 1	.....

Q2	Show how to connect bias voltages between the gate and source of the JFETs in Figure  (a) (b)
Sol 2	…… …… …… …… …… …… …… …… …… …… …… …… …… …… …… …… …… ……

Q3	A certain n-channel JFET is biased such that $V_{GS} = -2$ V. What is the value of $V_{GS(off)}$ if V_P is specified to be 6 V? Is the device on?
Sol 3	.....

Q4	A certain p-channel JFET has a $V_{GS(off)} = 6$ V. What is I_D when $V_{GS} = 8$ V?
Sol 4	.....

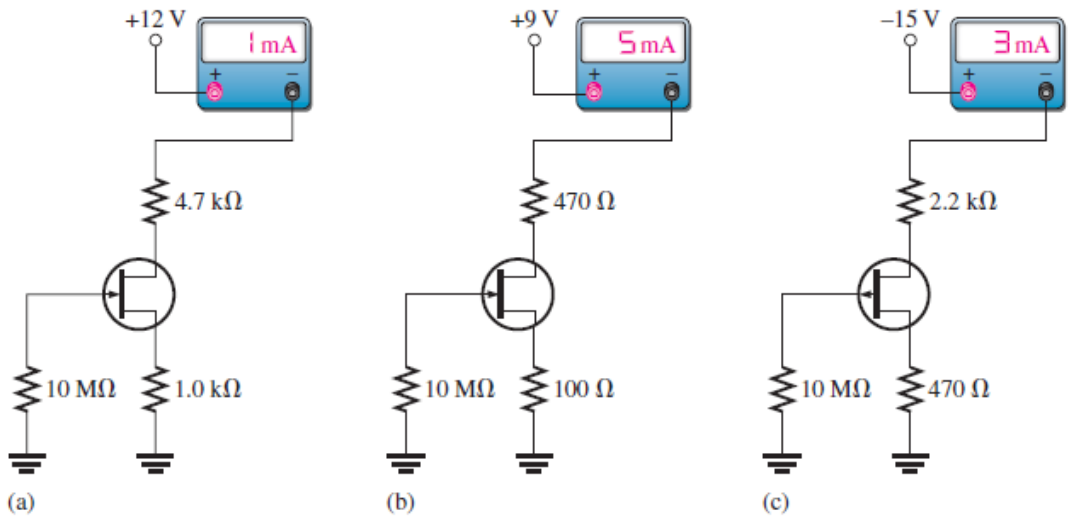
Q5	The following parameters are obtained from a certain JFET datasheet: $V_{GS(off)} = -8$ V and $I_{DSS} = 5$ mA. Determine the values of I_D for each value of V_{GS} ranging from 0 V to −8 V in 1 V steps. Plot the transfer characteristic curve from these data.
Sol 5	.....

Q6	For a particular JFET, $g_{m0} = 3200\ \mu\text{S}$. What is g_m when $V_{GS} = -4$ V, given that $V_{GS(off)} = -8$ V?
Sol 6	.....

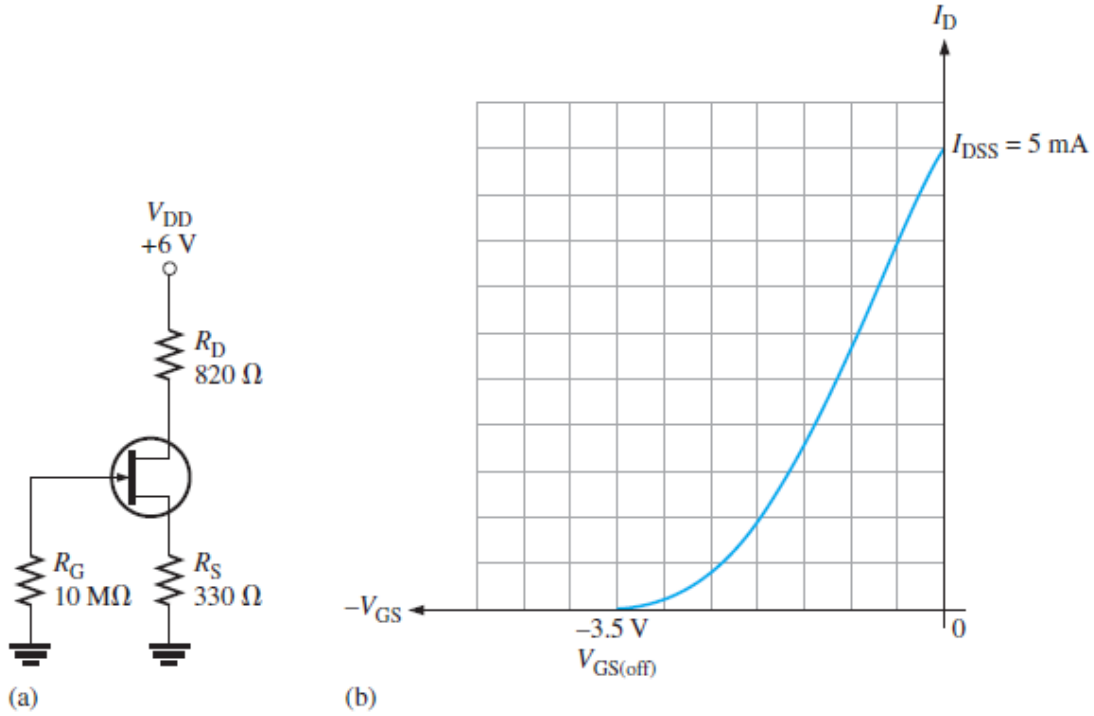
Q7	A p-channel JFET datasheet shows that $I_{GSS} = 5$ nA at $V_{GS} = 10$ V. Determine the input resistance.
Sol 7	.....

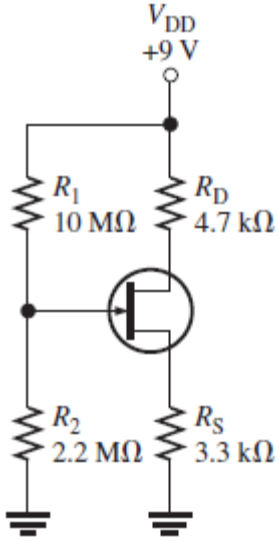
Q8	An n-channel self-biased JFET has a drain current of 12 mA and a 100 Ω source resistor. What is the value of V_{GS}?
Sol 8	.....

Q9	Determine the value of R_S required for a self-biased JFET to produce $I_D = 2.5$ mA when $V_{GS} = -3$ V.
Sol 9	.....

Q10	For each circuit in Figure , determine V_{DS} and V_{GS}. 
Sol 10	.....

Q11	Set up a midpoint bias for a JFET with $I_{DSS} = 14$ mA and $V_{GS(off)} = -10$ V. Use a 24 V dc source as the supply voltage. Show the circuit and resistor values. Indicate the values of I_D, V_{GS}, and V_{DS}.
Sol 11	.....

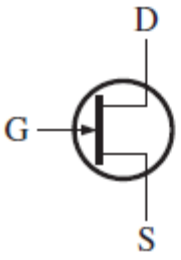
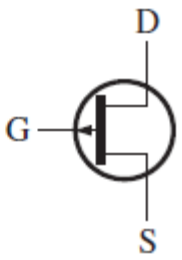
Q12	Graphically determine the Q-point for the circuit in Figure (a) using the transfer characteristic curve in Figure (b). 
Sol 12	…… …… …… …… …… …… …… …… …… …… ……

Q13	 Given that the drain-to-ground voltage in Figure is 5 V, determine the Q-point of the circuit.
Sol 13	…… …… …… …… …… …… …… …… …… …… …… …… …… …… ……

Q14	A certain JFET is biased in the ohmic region at $V_{DS} = 0.8$ V and $I_D = 0.20$ mA. What is the drain-to-source resistance?
Sol 14	.....

Q15	Determine the transconductance of a JFET biased at the origin given that $g_{m0} = 1.5$ mS, $V_{GS} = -1$ V, and $V_{GS(off)} = -3.5$ V.
Sol 15	.....

Q16	The V_{GS} of a *p*-channel JFET is increased from 1 V to 3 V. **(a)** Does the depletion region narrow or widen? **(b)** Does the resistance of the channel increase or decrease?
Sol 16	..... **(a)** Narrows **(b)** Increases .....

Q17	. Draw the schematic diagrams for a *p*-channel and an *n*-channel JFET. Label the terminals.
Sol 17	 *n*–channel  *p*–channel

Q18	A JFET has a specified pinch-off voltage of 5 V. When $V_{GS} = 0$, what is V_{DS} at the point where the drain current becomes constant?
Sol 18	..... 5 V .....

Q19	A certain JFET datasheet gives $V_{GS(off)} = -8$ V and $I_{DSS} = 10$ mA. When $V_{GS} = 0$, what is I_D for values of V_{DS} above pinch off? $V_{DD} = 15$ V.
Sol 19	..... 10 mA .....

Q20	The JFET in Figure has a $V_{GS(off)} = -4$ V. Assume that you increase the supply voltage, V_{DD}, beginning at zero until the ammeter reaches a steady value. What does the voltmeter read at this point?
Sol 20	..... 4 V .....

Q21	The following parameters are obtained from a certain JFET datasheet: $V_{GS(off)} = -8$ V and $I_{DSS} = 5$ mA. Determine the values of I_D for each value of V_{GS} ranging from 0 V to −8 V in 1 V steps. what value of V_{GS} is required to set up a drain current of 2.25 mA?
Sol 21	.... −2.63 V ....

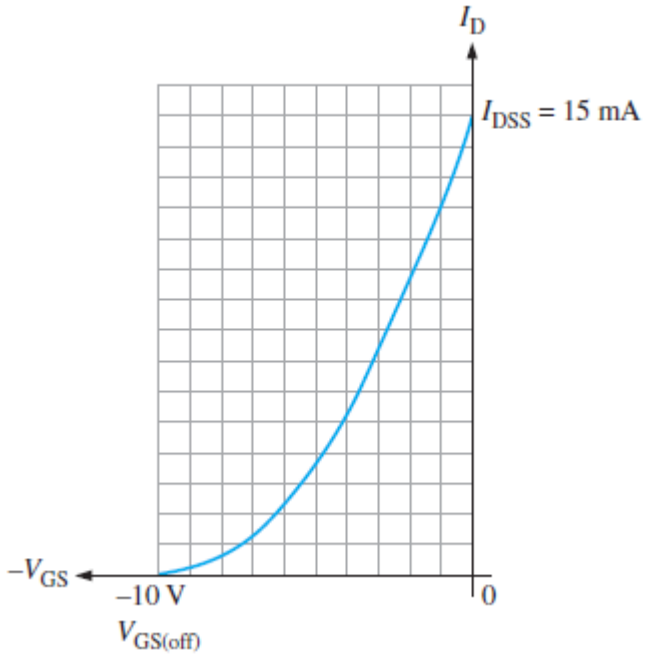
Q22	Determine the forward transconductance of a JFET biased at $V_{GS} = -2$ V. From the datasheet, $V_{GS(off)} = -7$ V and $g_m = 2000\ \mu$S at $V_{GS} = 0$ V. Also determine the forward transfer conductance, g_{fs}.
Sol 22	..... $g_m = 1429\ \mu\text{S}, g_{fs} = 1429\ \mu\text{S}$ .....

Q23	Using Equation , plot the transfer characteristic curve for a JFET with $I_{DSS} = 8$ mA and $V_{GS(off)} = -5$ V. Use at least four points. $$I_D \cong I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$
Sol23	$V_{GS} = 0\text{ V}, I_D = 8\text{ mA}$ $V_{GS} = -1\text{ V}, I_D = 5.12\text{ mA}$ $V_{GS} = -2\text{ V}, I_D = 2.88\text{ mA}$ $V_{GS} = -3\text{ V}, I_D = 1.28\text{ mA}$ $V_{GS} = -4\text{ V}, I_D = 0.320\text{ mA}$ $V_{GS} = -5\text{ V}, I_D = 0\text{ mA}$

Q24	Determine the value of R_S required for a self-biased JFET to produce a V_{GS} of -4 V when $I_D = 5$ mA.
Sol 24	800 Ω

Q25	$I_{DSS} = 20$ mA and $V_{GS(off)} = -6$ V for a particular JFET. (a) What is I_D when $V_{GS} = 0$ V? (b) What is I_D when $V_{GS} = V_{GS(off)}$? (c) If V_{GS} is increased from -4 V to -1 V, does I_D increase or decrease?
Sol 25	(a) 20 mA (b) 0 A (c) Increases

Q26



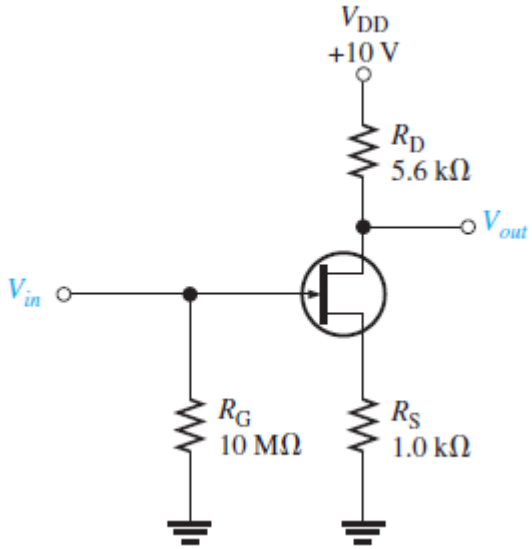
Using the curve in Figure , determine the value of R_S required for a 9.5 mA drain current.

Sol 26

211 Ω

Q27

Determine the total input resistance in Figure $I_{GSS} = 20$ nA at $V_{GS} = -10$ V.

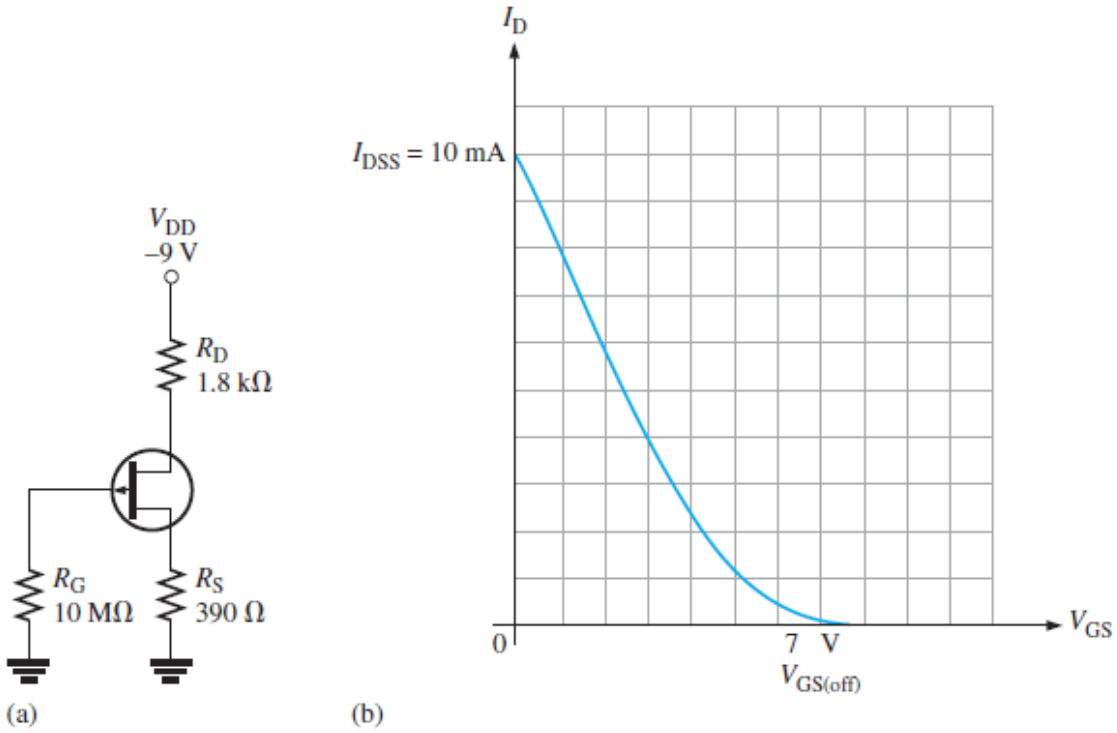


Sol 27

9.80 MΩ

Q28

Find the Q-point for the *p*-channel JFET circuit in Figure

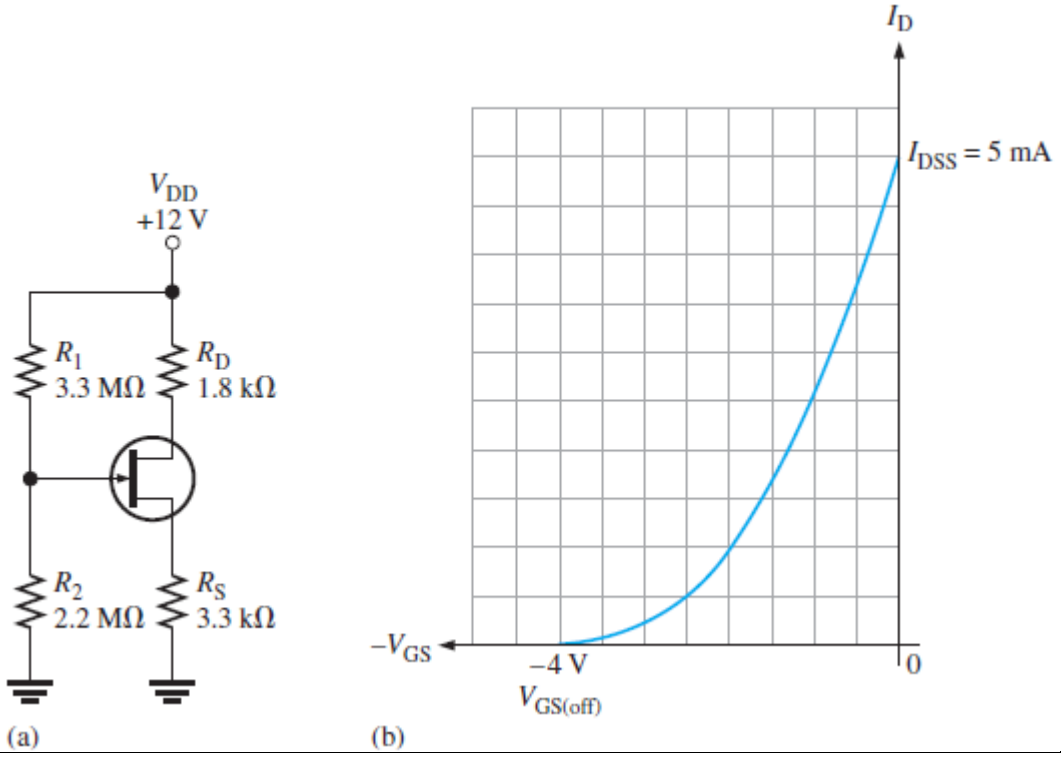


Sol 28

..... $I_D \cong 5.3$ mA, $V_{GS} \cong 2.1$ V .....

Q29

. Find the Q-point values for the JFET with voltage-divider bias in Figure



Sol 29

..... $I_D \cong 1.9\,\text{mA}, V_{GS} \cong -1.5\,\text{V}$ .....