Lecture (08.02)
The JFET

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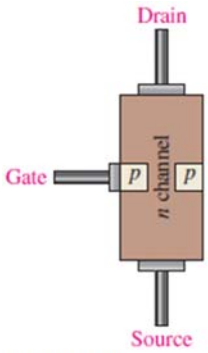
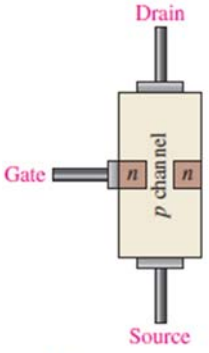
JFET **Basic Structure**

- Figure shows the basic structure of an *n*-channel JFET (junction field-effect transistor).
- Wire leads are connected to each end of the *n*-channel; the **drain** is at the upper end, and the **source** is at the lower end.
- Two *p*-type regions are diffused in the *n*-type material to form a **channel,** and both *p*-type regions are connected to the **gate** lead.
- For simplicity, the gate lead is shown connected to only one of the *p* regions.
- A *p*-channel JFET is shown in Figure



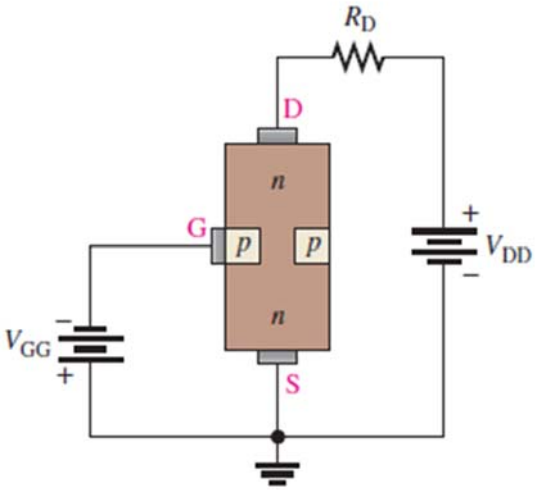
(a) *n* channel



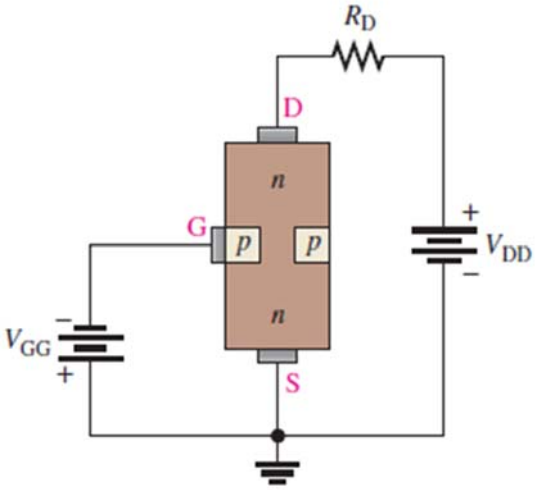
(b) *p* channel

Basic Operation

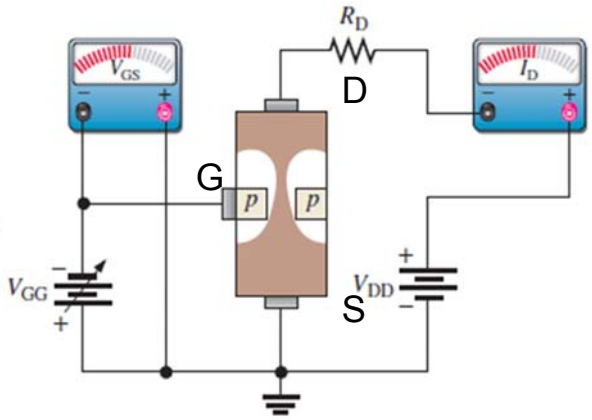
- To illustrate the operation of a JFET, Figure shows dc bias voltages applied to an *n*-channel device.
- *V*DD provides a drain-to-source voltage and supplies current from drain to source.
- *V*GG sets the reverse-bias voltage between the gate and the source, as shown.



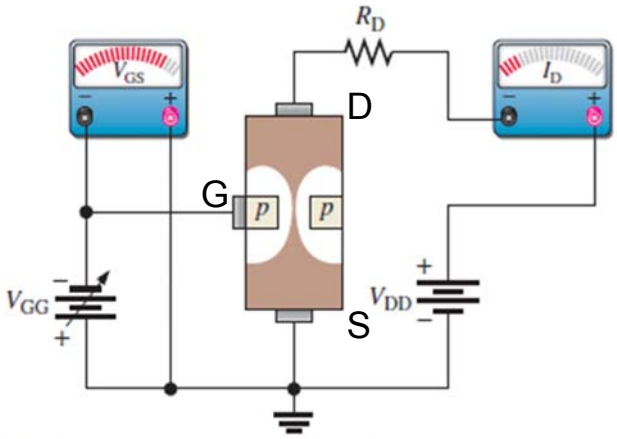
- a negative gate voltage produces a depletion region along the *pn* junction, which extends into the *n* channel and thus increases its resistance by restricting the channel width.
- The channel width and thus the channel resistance can be controlled by varying the gate voltage, thereby controlling the amount of drain current, *I*D.



- The white areas represent the depletion region created by the reverse bias.
- It is wider toward the drain end of the channel because the reverse-bias voltage between the gate and the drain is greater than that between the gate and the source



(a) JFET biased for conduction



(b) Greater V_{GG} narrows the channel (between the white areas) which increases the resistance of the channel and decreases I_D.

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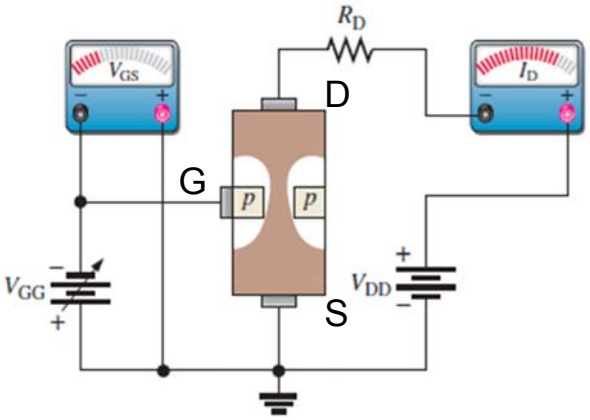
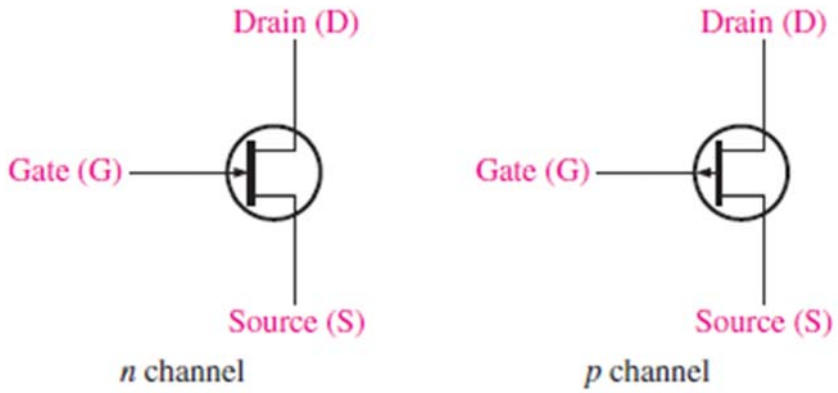


(c) Less V_{GG} widens the channel (between the white areas) which decreases the resistance of the channel and increases I_D.

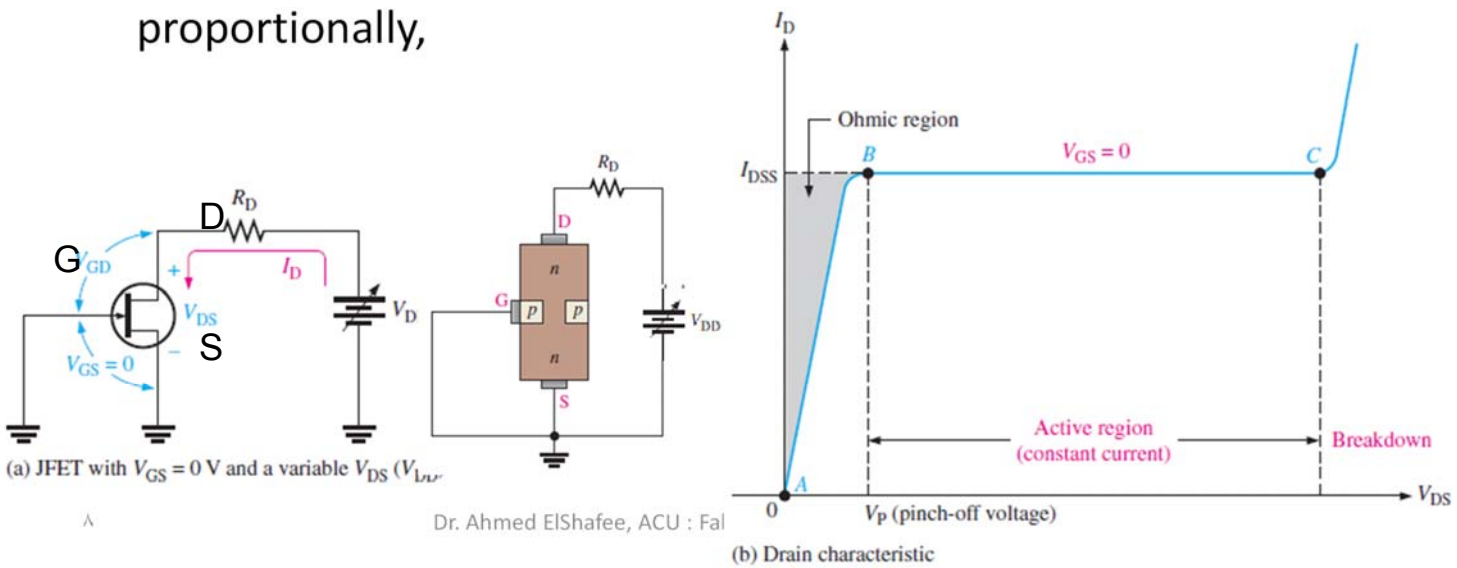
JFET Symbols

- The schematic symbols for both *n*-channel and *p*-channel JFETs are shown in Figure



FET characteristic and perameters

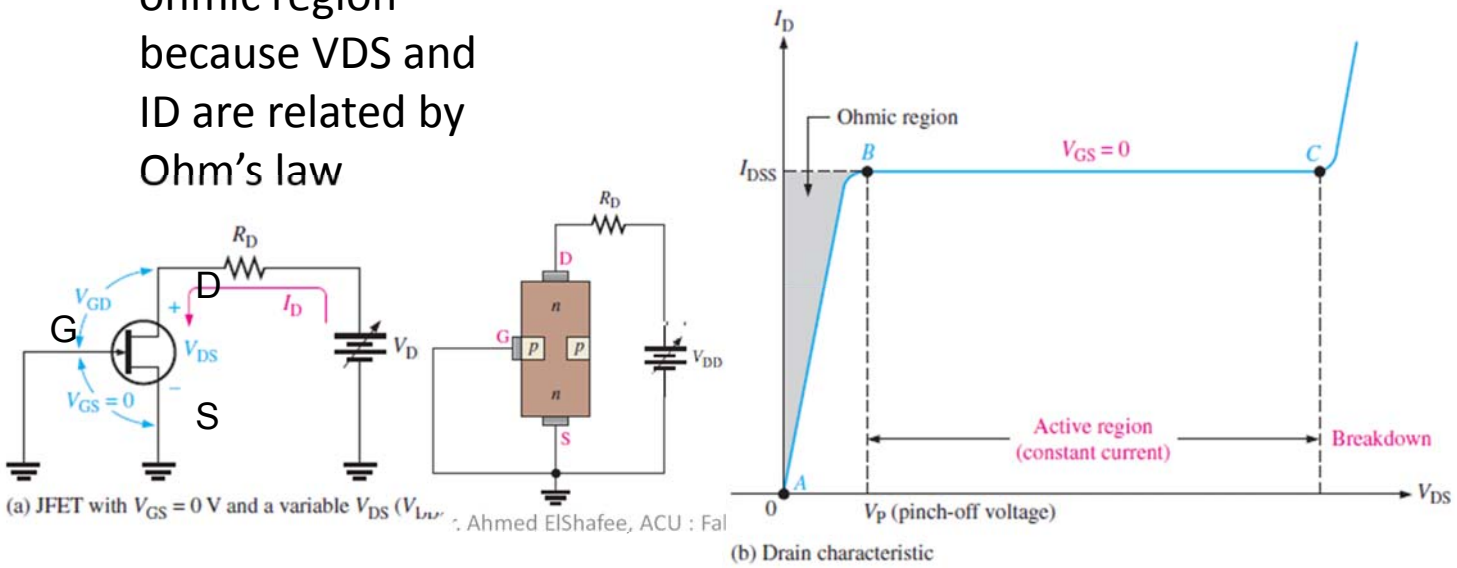
- The JFET operates as a voltage-controlled, constant-current device.
- (*V*GS = 0 V), gate to the source both are grounded.
- As *V*DD (and thus *V*DS) is increased from 0 V, *I*D will increase proportionally,



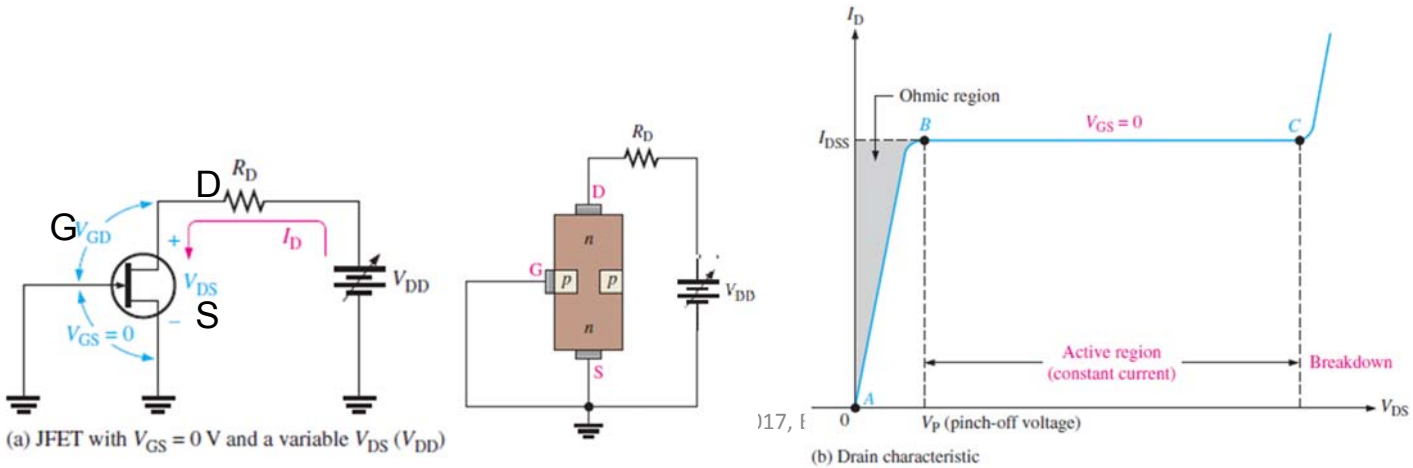
(a) JFET with $V_{GS} = 0$ V and a variable V_{DS} (V_{DD})

(b) Drain characteristic

- In this area, the channel resistance is essentially constant because the depletion region is not large enough to have significant effect
- This is called the ohmic region because VDS and ID are related by Ohm's law

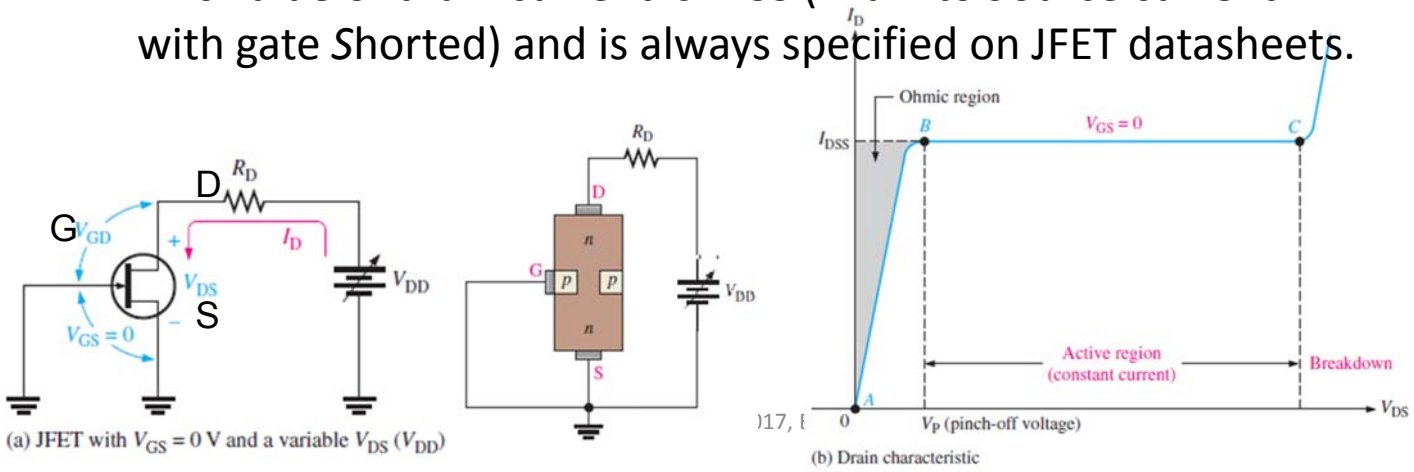


- At point *B,* enters the active region where *I*D becomes essentially constant.
- As *V*DS increases from point *B* to point *C*, the reverse-bias voltage from gate to drain (*V*GD) produces a depletion region large enough to offset the increase in *V*DS, thus keeping *I*D relatively constant.



Pinch-Off Voltage

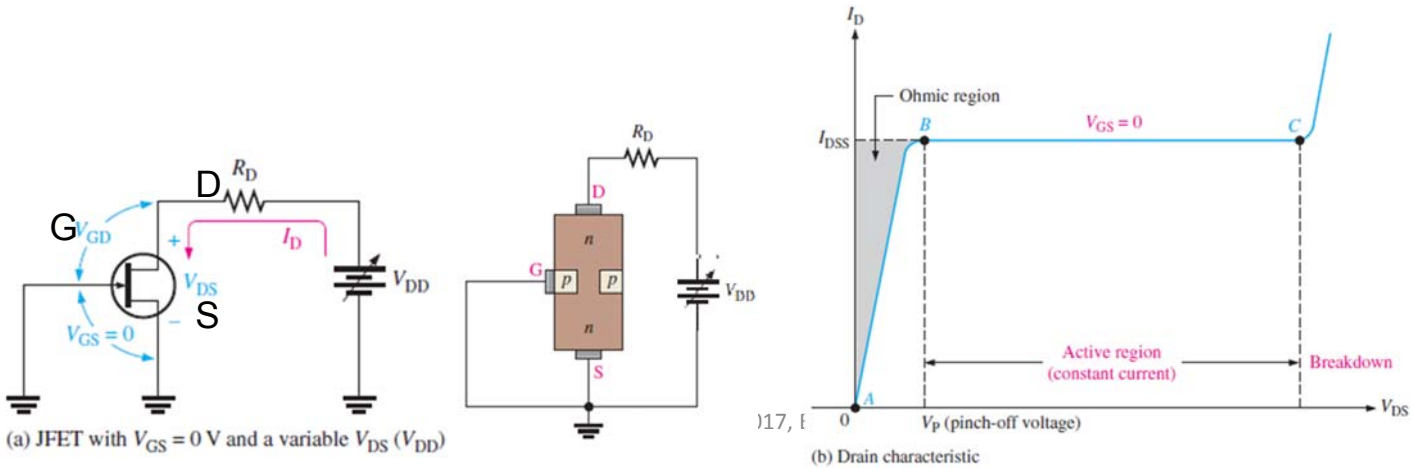
- For *V*GS =0 V, the value of *V*DS at which *I*D becomes essentially constant, point *B* on the is the **pinch-off voltage,** *V*P.
- For a given JFET, *V*P has a fixed value. a continued increase in *V*DS above the pinchoff voltage produces an almost constant drain current.
- This value of drain current is *I*DSS (*D*rain to *S*ource current with gate *S*horted) and is always specified on JFET datasheets.



(a) JFET with $V_{GS} = 0$ V and a variable V_{DS} (V_{DD})

(b) Drain characteristic

- *I*DSS is the *maximum* drain current that a specific JFET can produce regardless of the external circuit, and it is always specified for the condition, *V*GS 0 V.

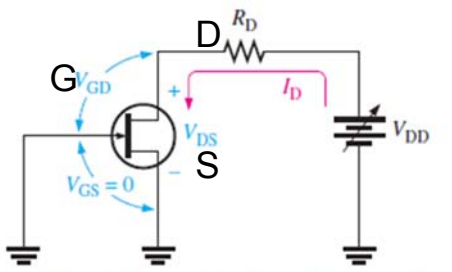


(a) JFET with $V_{GS} = 0$ V and a variable V_{DS} (V_{DD})

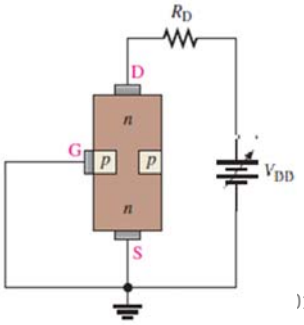
(b) Drain characteristic

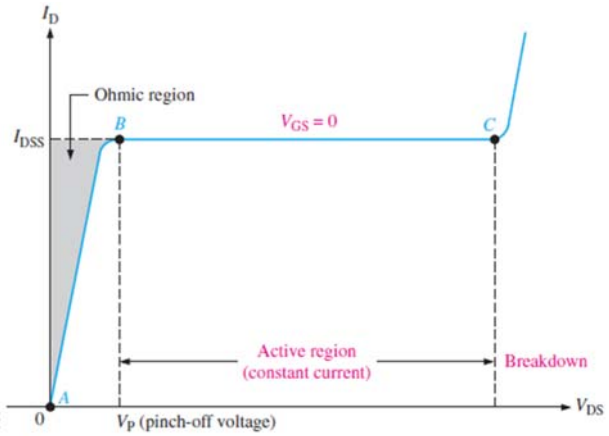
Breakdown

- **breakdown** occurs at point *C* when *I*D increase very rapidly with any further increase in *V*DS.
- Breakdown can result in irreversible damage to the device, so JFETs are always operated below breakdown and within the active region (constant current)

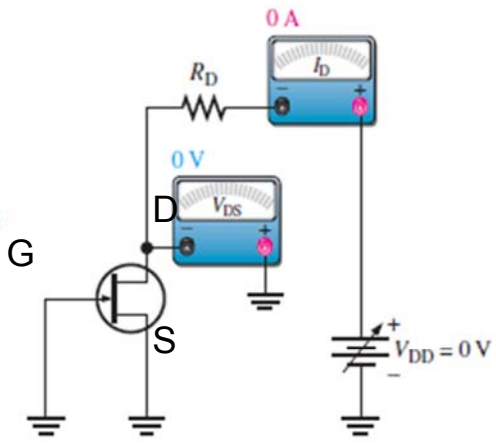


(a) JFET with $V_{GS} = 0$ V and a variable V_{DS} (V_{DD})

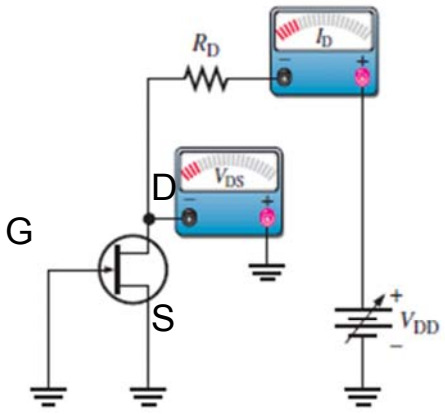




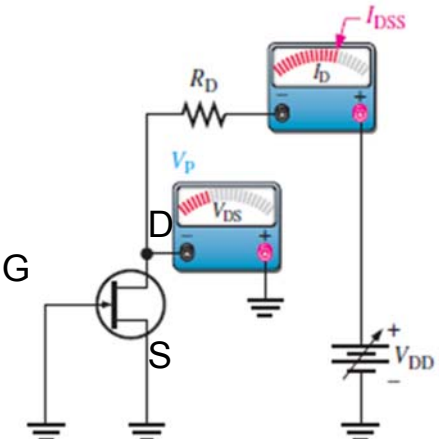
(b) Drain characteristic



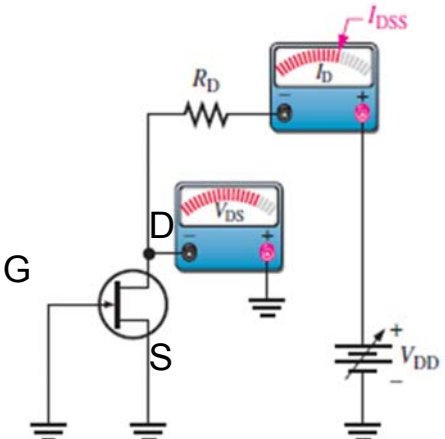
(a) When $V_{DS} = 0$, $I_D = 0$.



(b) I_D increases proportionally with V_{DS} in the ohmic region.



(c) When $V_{DS} = V_P$, I_D is constant and equal to I_{DSS}.



(d) As V_{DS} increases further, I_D remains at I_{DSS} until breakdown occurs.


Thanks,..
See you next week (ISA),…