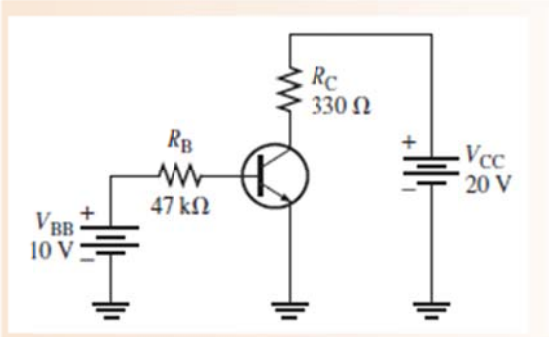
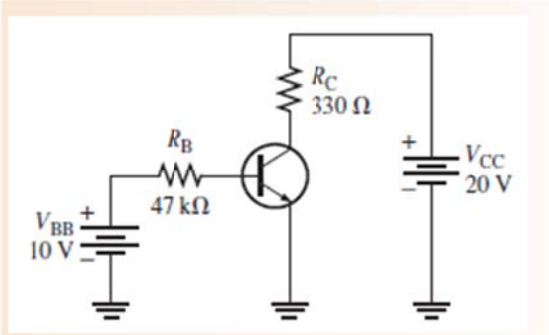
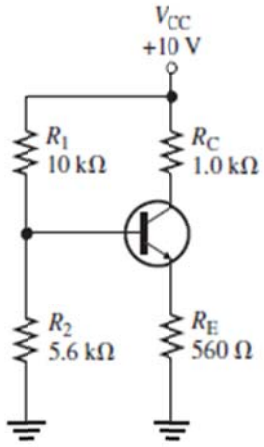
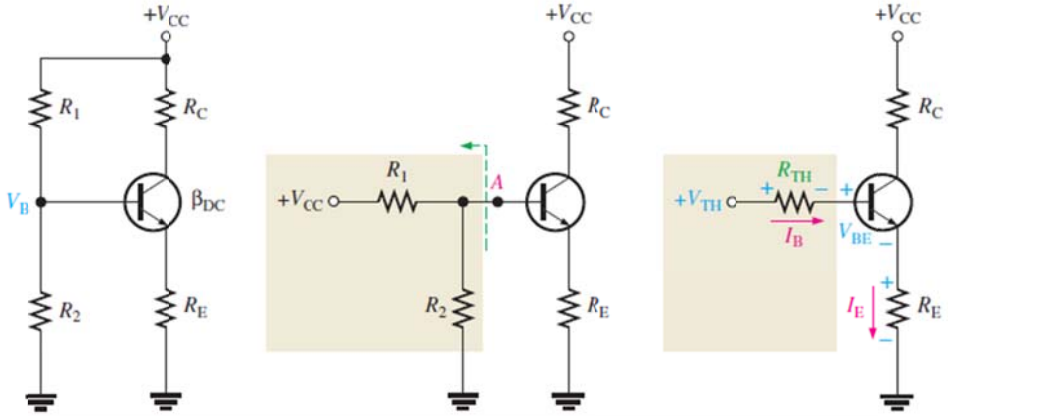
Electronic Circuits II – Tutorial 01

T & F

1	The linear region of a transistor's operation lies between saturation and cutoff.	T
2	Voltage-divider bias is rarely used.	F
3	Input resistance at the base of the transistor can affect voltage-divider bias.	T
4	Stiff voltage-divider bias is essentially independent of base loading.	T

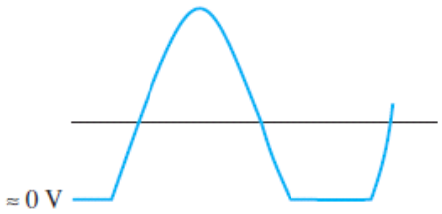
MCQ

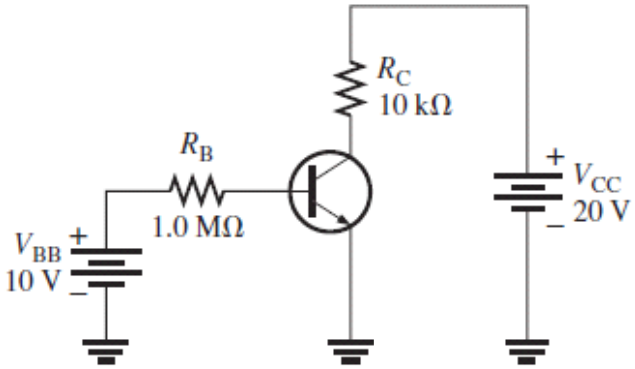
#	Question	
1	If VBB in Figure is increased, the Q-point value of collector current will  (a) increase (b) decrease (c) not change	a
2	If VBB in Figure is increased, the Q-point value of VCE will  (a) increase (b) decrease (c) not change	b

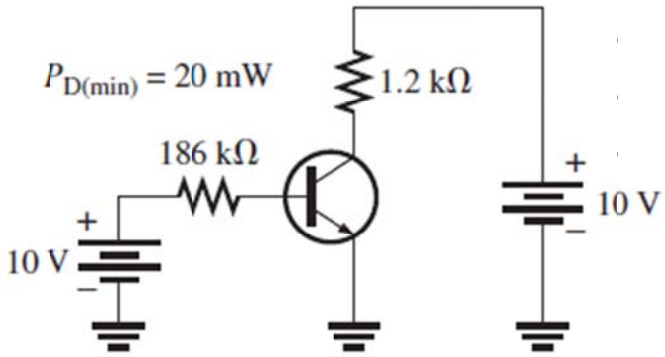
3	If the value of R2 in Figure is reduced, the base voltage will  (a) increase (b) decrease (c) not change	b
4	The maximum value of collector current in a biased transistor is (a) $\beta_{DC}I_B$ (b) $I_{C(sat)}$ (c) greater than I_E (d) $I_E - I_B$	b
5	If a sinusoidal voltage is applied to the base of a biased *npn* transistor and the resulting sinusoidal collector voltage is clipped near zero volts, the transistor is (a) being driven into saturation (b) being driven into cutoff (c) operating nonlinearly (d) answers (a) and (c) (e) answers (b) and (c)	d
6	 In a voltage-divider biased transistor circuit such as in Figure , $R_{IN(BASE)}$ can generally be neglected in calculations when (a) $R_{IN(BASE)} > R_2$ (b) $R_2 > 10R_{IN(BASE)}$ (c) $R_{IN(BASE)} > 10R_2$ (d) $R_1 \ll R_2$	c

7	Voltage-divider bias (a) cannot be independent of β_{DC} (b) can be essentially independent of β_{DC} (c) is not widely used (d) requires fewer components than all the other method	b

Problems

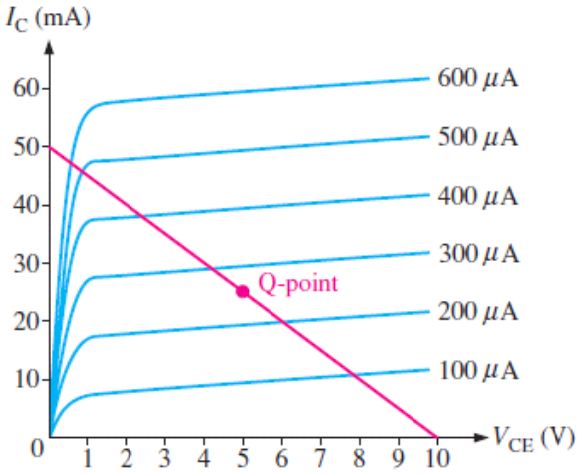
Q1	The output (collector voltage) of a biased transistor amplifier is shown in Figure . Is the transistor biased too close to cutoff or too close to saturation? 
Sol 1	.....

Q 2	Determine the intercept points of the dc load line on the vertical and horizontal axes of collector-characteristic curves for the circuit in Figure 
Sol 2	..... $V_{CE} = 20\text{ V}; I_{C(sat)} = 2\text{ mA}$ .....

Q3	Design a biased-transistor circuit using $V_{BB} = V_{CC} = 10$ V for a Q-point of $I_C = 5$ mA and $V_{CE} = 4$ V. Assume $\beta_{DC} = 100$. The design involves finding R_B, R_C, and the *minimum* power rating of the transistor. (The actual power rating should be greater.) Sketch the circuit.
Sol 3	

Q4

▶ FIGURE



From the collector characteristic curves and the dc load line in Figure , determine the following:

(a) Collector saturation current

(b) V_{CE} at cutoff

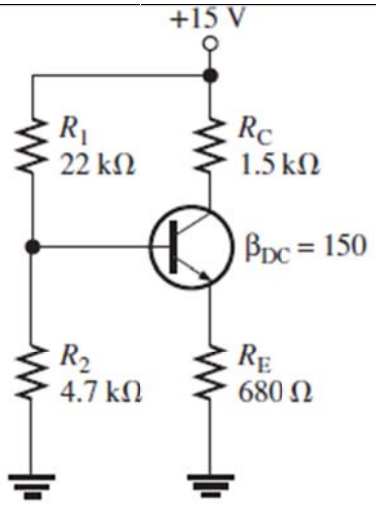
(c) Q-point values of I_B, I_C, and V_{CE}

Sol 4

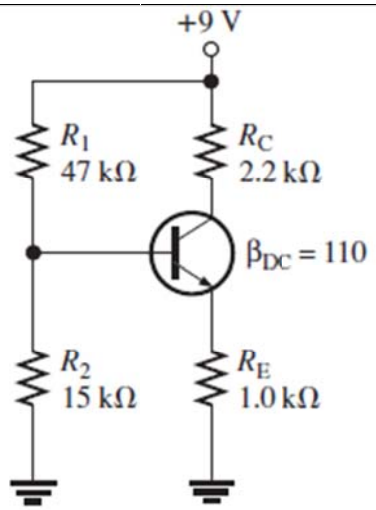
(a) $I_{C(sat)} = 50\ \text{mA}$

(b) $V_{CE(CUTOFF)} = 10\ \text{V}$

(c) $I_B = 250\ \mu\text{A}; I_C = 25\ \text{mA}; V_{CE} = 5\ \text{V}$

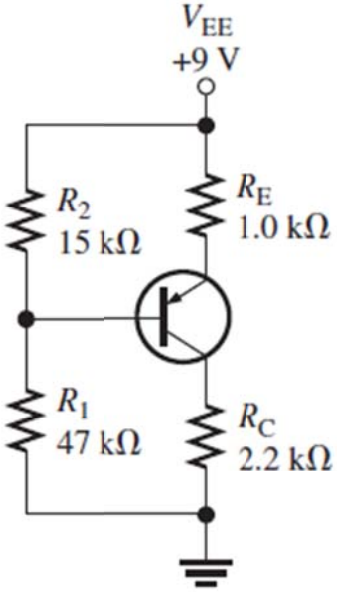
Q5	 What is the minimum value of β_{DC} in Figure that makes $R_{IN(BASE)} \geqq 10R_2$?
Sol 5	…… …… …… …… …… …… ……

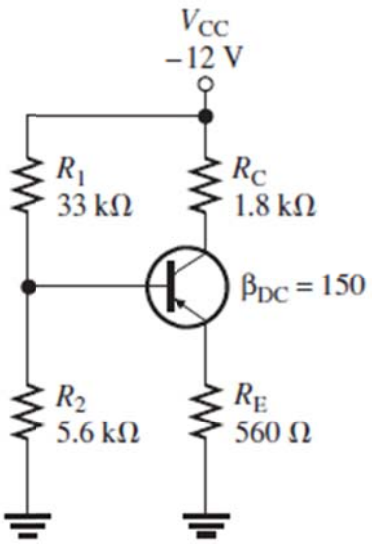
Q6



Show the connections required to replace the transistor in Figure ' with a *pnp* device.

Sol 6



Q7	 Determine the following in Figure : (a) Q-point values (b) The minimum power rating of the transistor
Sol 7	…… …… …… …… …… …… ……